REMARKS

Claims 1-14, 16-21 and 23-40 are pending. Claims 1-14, 16-21 and 34-40 have been allowed. Claims 23, 25, 27, 29-30 and 32-33 have been amended. In view of the following, all of the claims are in condition for allowance. But if after considering this response the Examiner does not agree that all of the claims are in condition for allowance, then the Examiner is requested to schedule an interview with the Applicants' attorney to further prosecution of this application.

Rejection of Claims 23-26 Under 35 U.S.C. § 102(b) As Being Anticipated by Biggs et al. (US 6,128,716)

Claim 23

Claim 23, as amended, recites receiving an address strobe with a memory circuit, receiving a first address with the memory circuit during a data-transfer cycle, generating a second address with the memory circuit during the data-transfer cycle, comparing the first address to the second address with the memory circuit, and terminating the data-transfer cycle if the first address does not have a predetermined relationship to the second address.

For example, referring to FIGS. 3-5 and pages 5-11 of the present application, a column-address anticipation counter 14 receives an address strobe CAS, a comparator 18 compares a received external column address with an internal column address generated by the counter 14, and a column decoder 38 transfers data to/from a location of the array 30 residing at the internal column address. A control circuit 24 terminates this data-transfer cycle if the external column address does not have a predetermined relationship to the internal column address. For example, per the timing diagram of FIG. 3, the control circuit 24 may terminate the data-transfer cycle if the internal column address does not equal the external column address. It should be noted that this all occurs during a single data-transfer cycle t_{IPC} and within a memory circuit 26.

In contrast, Biggs does not disclose receiving an address strobe with a memory circuit, receiving a first address with the memory circuit during a data-transfer cycle, generating a second address with the memory circuit during the data-

transfer cycle, comparing the first address to the second address with the memory circuit, and terminating the data-transfer cycle if the first address does not have a predetermined relationship to the second address. Instead, Biggs simply discloses a DRAM 43 that receives address strobes RAS and CAS from a state machine 56 (FIG. 1). The DRAM 43 is the only component in Biggs that receives any kind of address strobe. However, the DRAM 43 is simply a memory array and is unable to generate an address or compare two addresses. In fact, the only components in Biggs that are capable of generating an address or comparing two addresses are located within a memory controller 42 (FIG. 1). The memory controller 42 is entirely separate from the DRAM 43, and does not receive any address strobes whatsoever. To the contrary, the memory controller 42 actually generates address strobes RAS and CAS instead of receiving them. Therefore, Biggs does not satisfy the limitations of claim 23.

Claims 24-26

Claims 24-26 are patentable by virtue of their dependency from independent claim 23.

Rejection of Claims 27-33 Under 35 U.S.C. § 102(b) As Being Anticipated by Ryan et al. (US 5,966,724)

Claim 27

Claim 27, as amended, recites loading a memory circuit with a predetermined value, receiving with the memory circuit during a data transfer cycle a first address from a source external to the memory circuit, comparing the first address to the predetermined value with the memory circuit, and terminating the data-transfer cycle if the first address has a predetermined relationship to the predetermined value.

For example, referring to FIGS. 3-5 and pages 5-11 of the patent application, a column-address anticipation counter 14 generates an internal column (first) address and data is transferred to or from the location in the array 30 at the internal column address. A comparator 18 compares the internal column address to a predetermined value loaded in the register/counter 16, and the control circuit 24 terminates the data-transfer cycle if the internal column address has a

predetermined relationship (*e.g.*, is equal) to the value stored in the register/counter 16. It should be noted that this all occurs during a single data-transfer cycle t_{IPC} and within a memory circuit 26.

In contrast, Ryan does not disclose loading a memory circuit with a predetermined value, receiving with the memory circuit during a data transfer cycle a first address from a source external to the memory circuit, comparing the first address to the predetermined value with the memory circuit, and terminating the data-transfer cycle if the first address has a predetermined relationship to the predetermined value. Instead, Ryan simply discloses a control circuitry 38 that contains an initial address latch and a comparator that compares the initial address (predetermined value) with "internally generated addresses" and terminates the burst access when a match occurs (FIG. 1; col. 5, lines 49-54). However, this is contrary to the limitations of claim 27 because the control circuitry 38 compares the initial address (predetermined value) to an address that is "internally generated" instead of an address that is received from a source external to the control circuitry 38. Even if the Examiner were to argue that the memory circuit is restricted to memory array 12 so that the addresses generated by the control circuitry 38 are external to the memory array 12, then the limitations of claim 27 are still not satisfied because the memory array 12 is itself unable to compare an address to a predetermined value. Therefore, Ryan does not satisfy the limitations of claim 27.

Claims 28-33

Claims 28-33 are patentable by virtue of their dependency from independent claim 27.

CONCLUSION

In light of the foregoing, all pending claims are in condition for allowance, which is respectfully requested.

In the event additional fees are due as a result of this amendment, you are hereby authorized to charge such payment to Deposit Account No. 08-2025.

If after considering this response the Examiner does not agree that all pending claims are in condition for allowance, the Examiner is requested to schedule an interview with the Applicants' attorney at (425) 455-5575 to further prosecution of this application.

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Respectfully Submitted,
GRAYBEAL JACKSON HALEY LLP

Bryan A. Santarelli
Attorney for Applicant
Registration No. 37,560
155 – 108th Ave. NE, Suite 350
Bellevue, WA 98004-5973
Phone: (425) 455-5575
Fax: (425) 455-1046
Email: bryans@graybeal.com